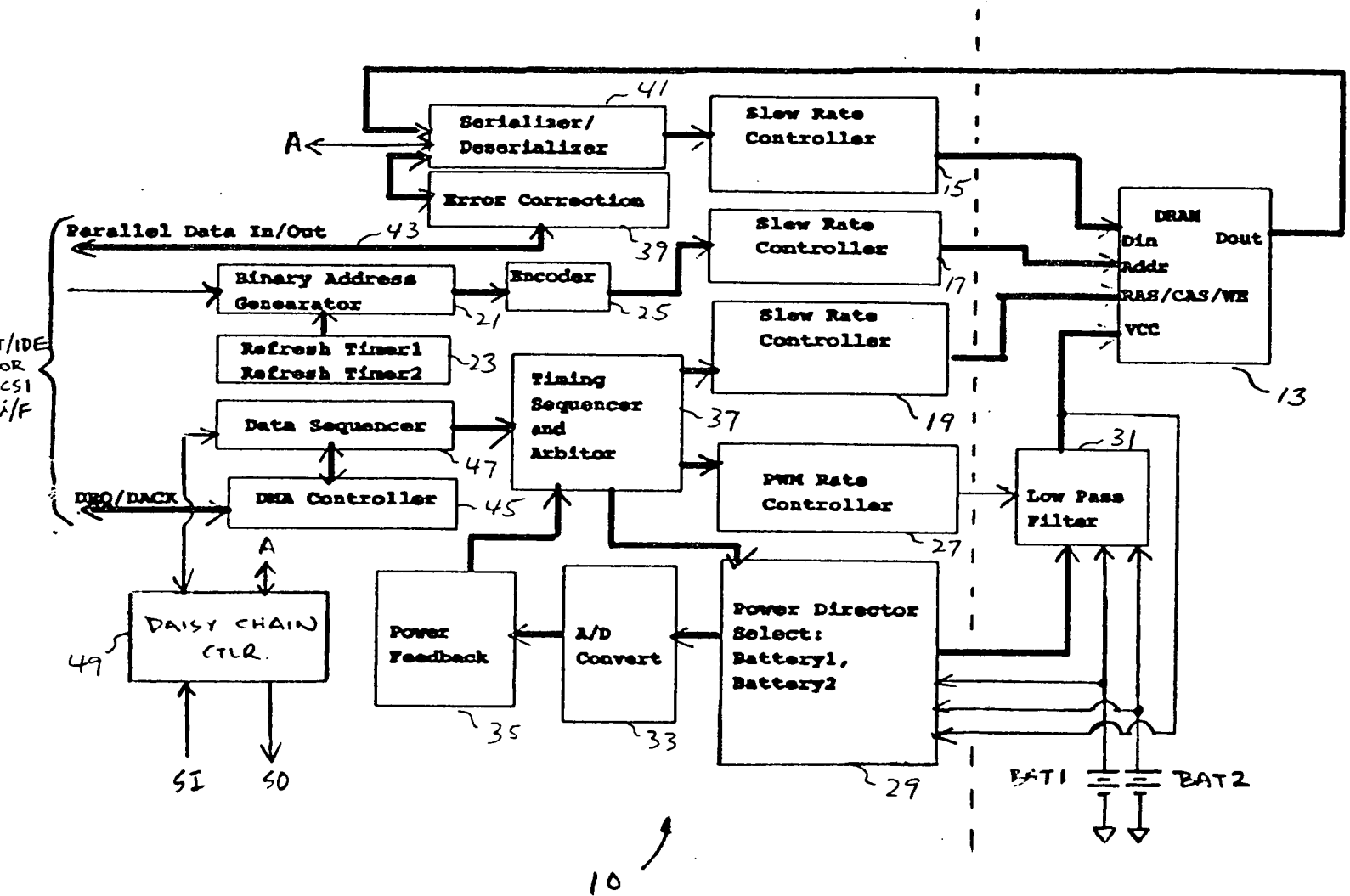


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Figure 1



Power Sequence

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Fig 2a

+5V
 +3V
 +2V
 +1.5V

RAM VCC

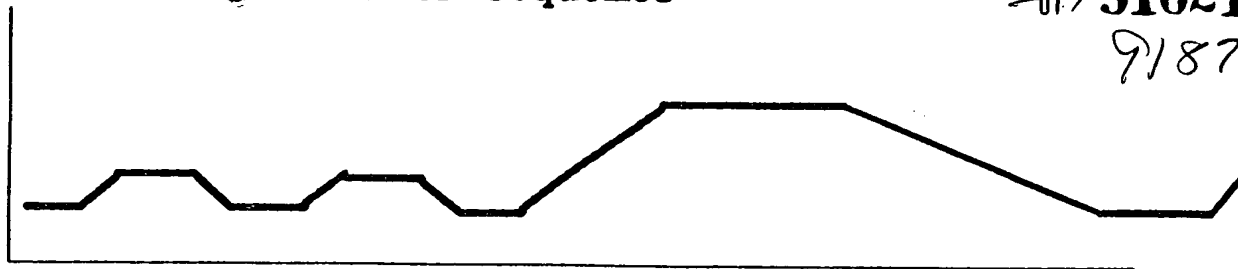


Fig 2b

Cycle

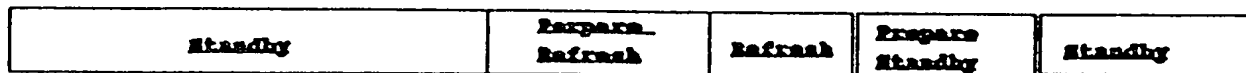


Fig 2c

+2.2V

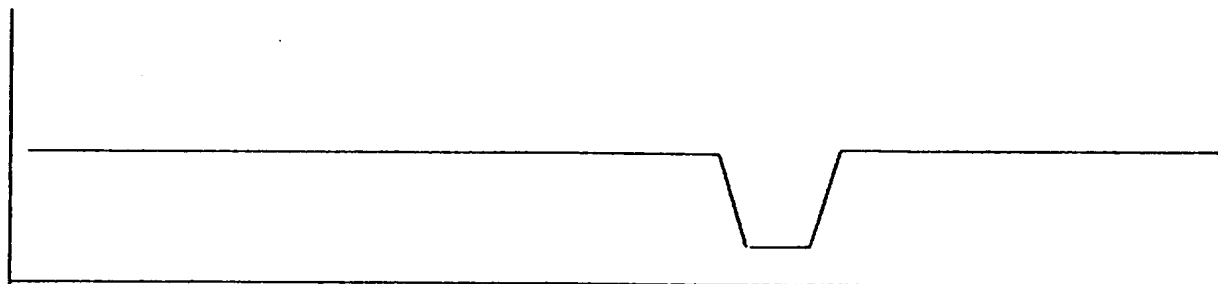


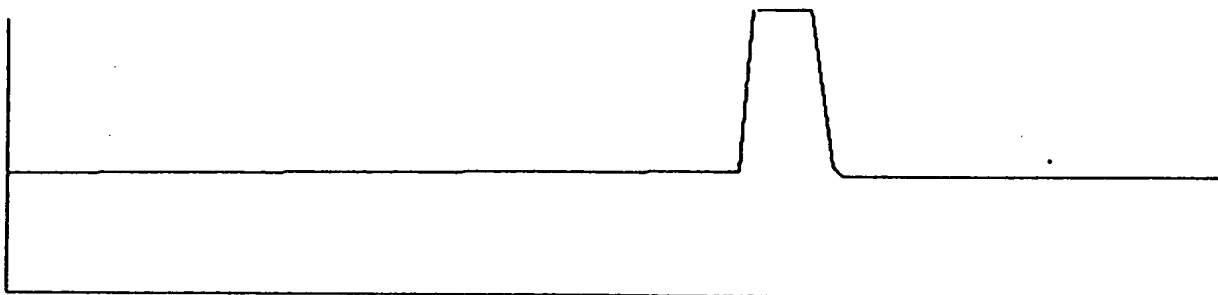
Fig 2d

1000

100

10

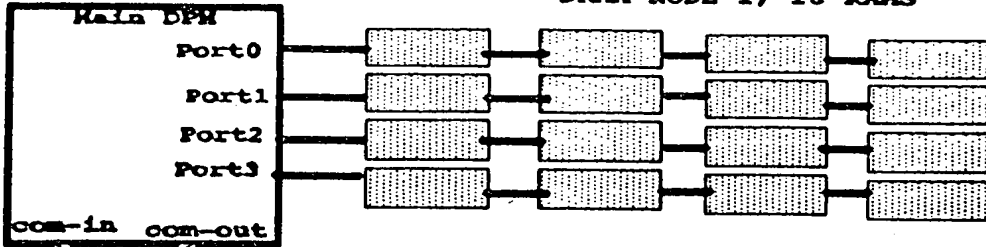
Current (mA)



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Dynamic Power Module

DRAM NODE 1, 16 RAMS



DRAM NODE 2, 16 RAMS

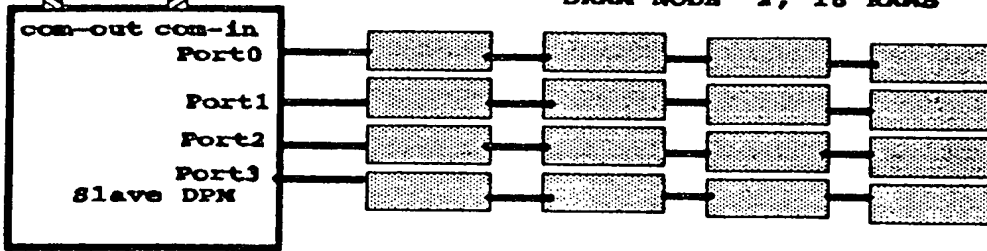


Fig 3

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Voltage across DRAMS For Four DRAMS

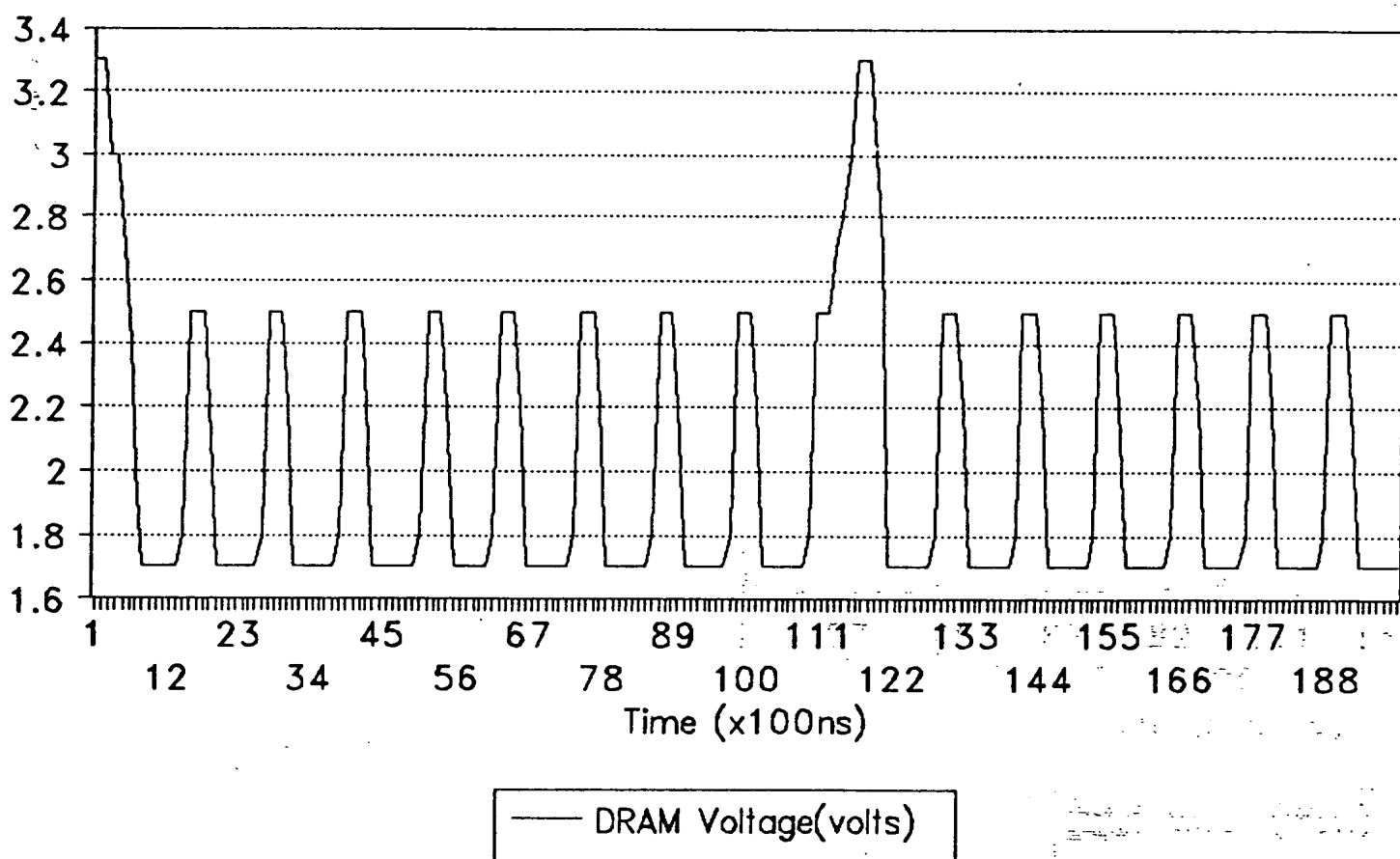


Fig 4

Power for Four Rams over one Period (Refresh access is included)

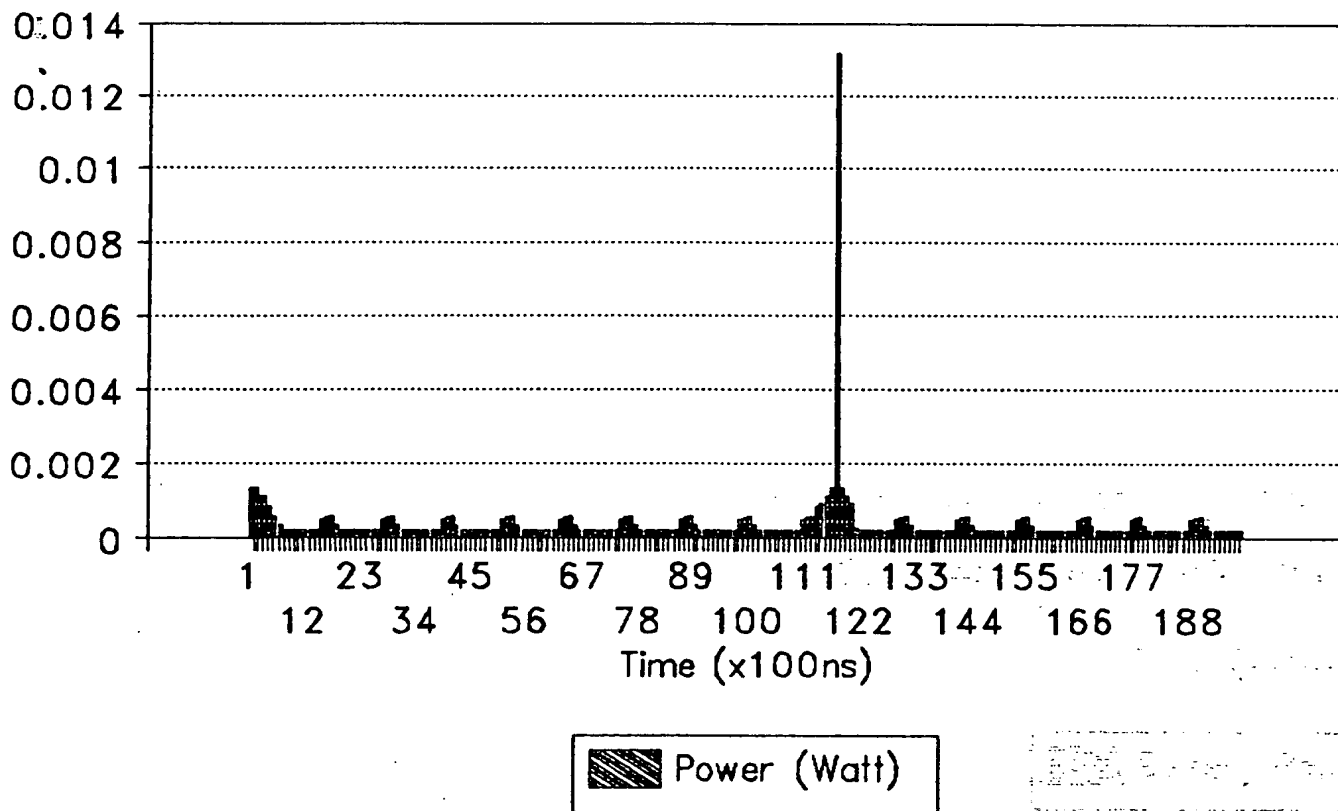


Fig 5

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Battery Power Consumed For Four DRAMs

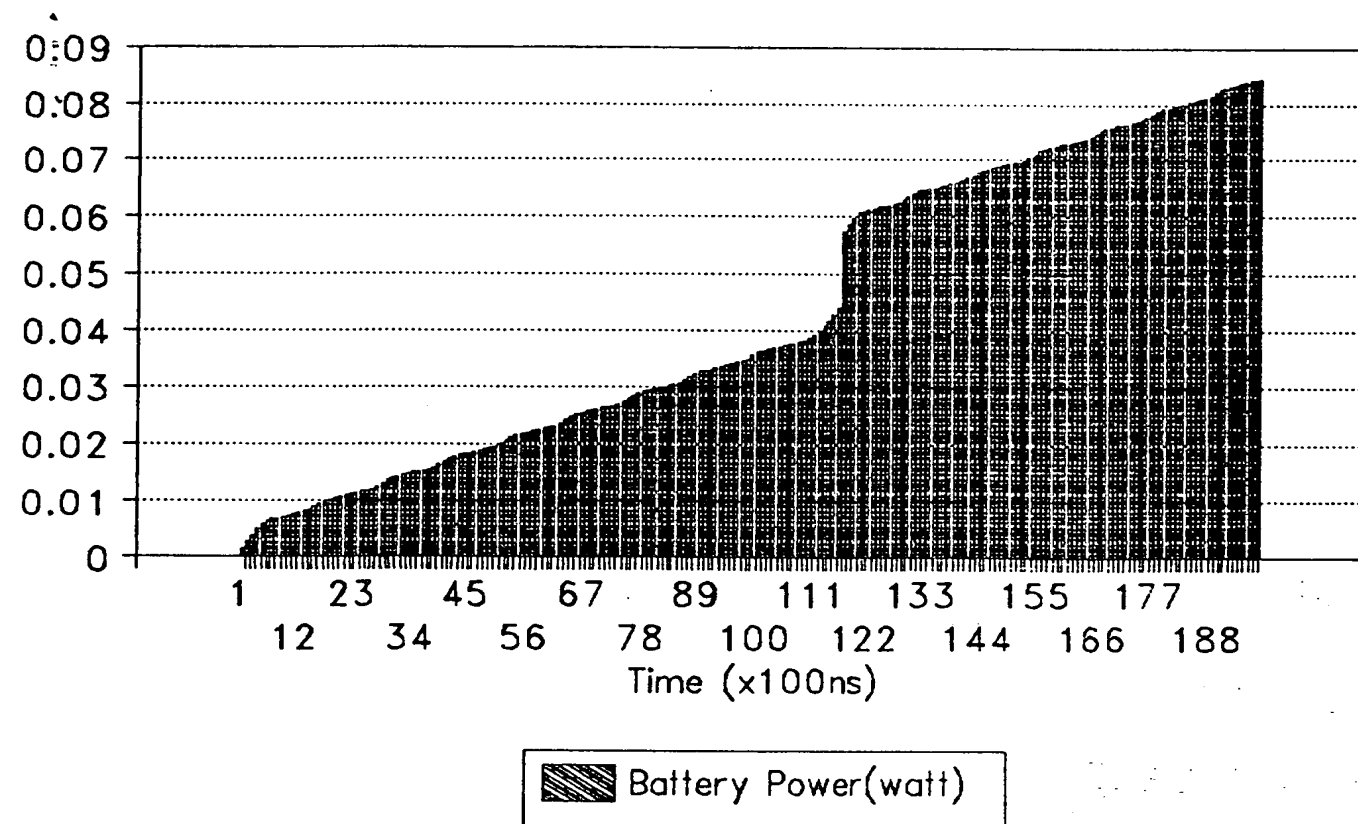


Fig 6

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Battery Life(50mA Hr), 8 DRAMS (Hot Standby Battery)

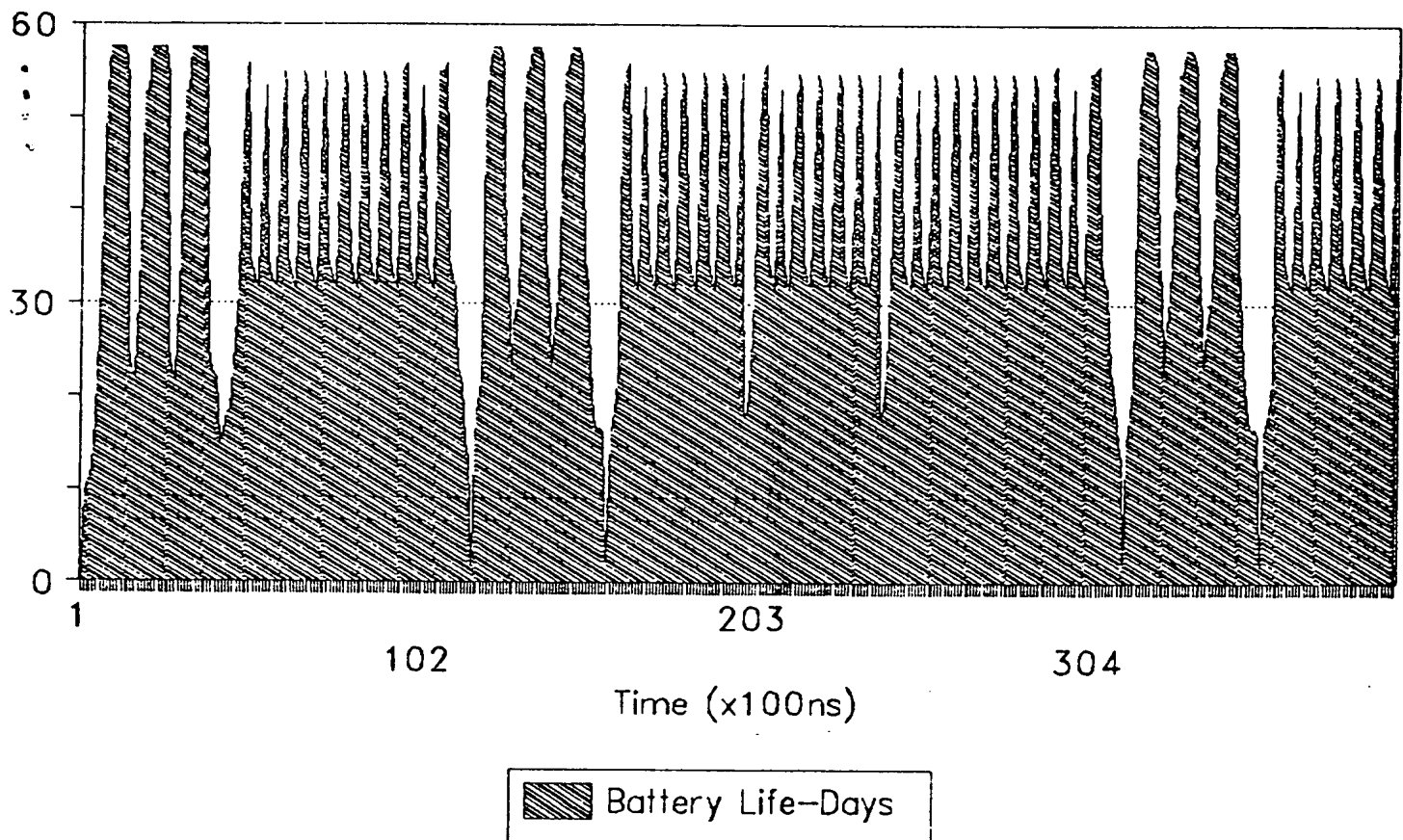


Fig 7